

# Reconfigurable Performance Measurement System-on-a-Chip for Baseband Wireless Algorithm Design and Verification

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**Abstract**—Modern wireless technology applies several powerful but complex techniques—such as multiple-antenna systems, orthogonal frequency division multiplexing, and capacity-approaching forward error correcting codes—to provide reliable broadband digital communications over the time-varying mobile radio channel. Such techniques appear in most recent wireless standards such as IEEE 802.11n Wi-Fi, IEEE 802.16 WiMax, and the Third Generation Partnership Project’s Long Term Evolution (3GPP LTE). Bit error rate simulation continues to be the workhorse design verification and performance optimization methodology; however, the growing complexity of modern wireless systems and the tendency of wireless standards to evolve even after product development has started, have greatly increased the required simulation times to the extent that software-based simulation is now the major bottleneck in wireless system development. This article describes how baseband performance verification of wireless systems can be accelerated by over four orders of magnitude using compact, accurate and high-throughput emulators implemented on reconfigurable field-programmable gate arrays (FPGAs).

**Index Terms**—Wireless communication, bit error rate simulation, radio fading channel, rapid prototyping, hardware accelerator, design verification.

## I. INTRODUCTION

Wireless communication systems have rapidly become an indispensable part of our modern lifestyle. Fig. 1 shows a simplified block diagram of a typical wireless system. At the transmitter (TX) side, the input data is passed through various upper layers and processed by one or more application processors before being passed to the physical (PHY) layer. The PHY layer is mainly responsible for transmitting and receiving binary digits over a noisy communication medium as reliably as possible. The baseband section at the PHY layer of the transmitter performs various signal processing functions including channel coding so that the receiver (RX) is able to correct most of the corrupted received signals. The digital baseband signal is then modulated and upconverted to a radio frequency (RF) signal, which is then amplified for transmission from the TX antenna. In a wireless communication system, the radio channel is the communication medium between the TX and the RX that carries information originating from higher layers as well as control signals for system synchronization and channel estimation. At the receiver side, the received signal is amplified, downconverted to a lower frequency and then demodulated to recover digital signals for further processing by the baseband section. The baseband

section in the receiver recovers the transmitted data using several signal processing stages including channel estimation, signal detection and channel decoding. The estimated data is then passed on to the upper layers of the protocol stack.

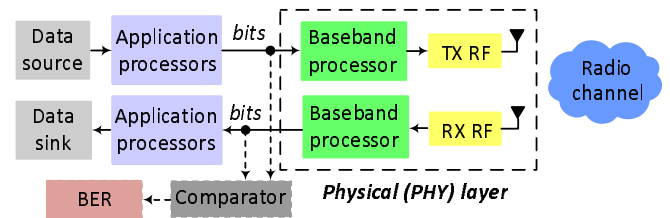


Fig. 1. Block diagram of a typical wireless system and BER measurement.

It is important to note that both the baseband section and the RF front-end of the PHY layer are subject to various impairments. For example, fixed-point implementation of the baseband signal processing algorithms introduces quantization error, and a variety of impairments are introduced by the RF front-end, such as phase and amplitude distortion from the non-linear power amplifier and phase noise from the local oscillators [1]. However, due to various electromagnetic propagation effects and the time-varying nature of the propagation environment, radio channel impairments have the most significant impact on the performance of wireless communication systems. Overcoming these impairments is a key objective of the PHY layer.

As shown in Fig. 1, at the PHY layer, the bit error rate (BER) metric, which is the ratio of errored bits to transmitted bits, is widely used to characterize the performance of receiver devices-under-test (DUT) over the expected range of signal-to-noise ratio (SNR) conditions. Since the BER properties are not in general amenable to analysis, Monte Carlo (MC) simulation techniques have been widely used to generate BER versus SNR characteristics. Unfortunately, the execution times of software-based MC simulations of the baseband layer on workstations can be extremely long for the following reasons:

- The PHY layer of modern broadband communication systems is significantly more complex than that of the preceding generations. For example, the emerging IEEE 802.11ac standard targets higher throughput by incorporating wider bandwidth and a greater number of transmitter and receiver

antennas compared to the preceding IEEE 802.11n standard. Software-based MC simulation of increasingly complex PHY layers over a continuously varying radio channel can take weeks or even months to accurately estimate the BER over the SNR range of interest. The required time can become prohibitively long especially for the fixed-point and bit-true simulations.

- Due to advances in communication techniques, the number of possible configurations in which products need to operate and hence be verified has increased significantly. For example, a wireless system should operate reliably in various radio propagation environments (e.g., indoor, urban, sub-urban, and rural), adapt to unpredictable channel conditions by changing its transmission scheme (e.g., different modulation and/or code rates), and select alternative detection techniques. Therefore, the performance of wireless systems must be evaluated under a large number of settings and options. As the number of possible configurations in emerging standards increases (e.g., more than 300 modulation and coding schemes are present in the IEEE 802.11n WLAN standard), software-based verification of emerging broadband communication systems has become the bottleneck to timely design and verification.

- For a communication system with a target error performance, there are typically many potential baseband solutions. Each solution can utilize a different combination of subsystem designs. Exploring the design space to achieve an optimized overall system solution that meets the target specifications typically involves evaluating a large number of options. Software-based performance verification of these potential solutions could be extremely slow, especially for modern communication systems with computationally-intensive signal processing.

Given the aggressive time schedules for developing new wireless products and very tight time-to-market constraints, designers must design and verify increasingly complex signal processing algorithms in very short design cycles. Speeding up the verification of new wireless systems, despite frequently changing standards, also poses major challenges for the test equipment vendors. A more practical approach for measuring the BER performance at the PHY layer is to use a hardware-based verification system. Hardware-based BER testers (BERTs) can dramatically accelerate the PHY layer performance measurement compared to software-based simulators, significantly reducing the verification time.

This article reviews challenges in the baseband design and verification of high capacity wireless communication systems. We describe a parameterizable hardware-accelerated performance measurement system for multiple-input multiple-output (MIMO) communication systems. This system utilizes accurate radio channel models to reproduce the statistical properties of MIMO propagation environments on a reconfigurable chip. The system can be easily parameterized to adapt to the specifications of emerging standards and is scalable to support various numbers of antennas and channel configurations.

## II. MODELING RADIO CHANNELS

As shown in Fig. 2, during transmission through the radio channel, a signal typically travels from the transmitter to the receiver along different propagation paths. Due to the processes of reflection, diffraction, and scattering from objects, multiple copies of the transmitted signal, called multipath signal components, arrive at the receive antenna via different paths with different time delays, amplitudes, and phases. The signal may also take the direct line-of-sight (LOS) path. If the propagation environment changes or if there is a relative motion between the transmit and receive antennas, each multipath signal component experiences a slight shift in frequency, called a Doppler shift [2].

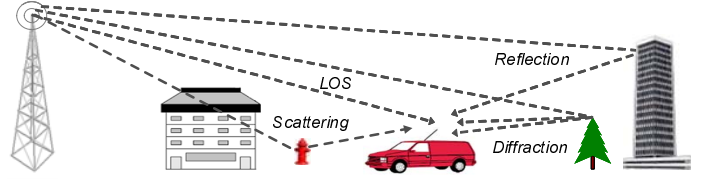


Fig. 2. A typical multipath fading channel.

Wireless communication systems must be designed to operate over radio channels for a wide variety of expected environments. The initial performance verification of a communication system at the early stages of the design cycle is performed based on the channel characteristics defined by the underlying wireless communication standard. Wireless standards usually specify a multipath fading channel using a power delay profile, which defines the average received power  $p_\ell$  and the arrival time  $\tau_\ell$  for  $L$  multipath components, where  $\ell = 0, \dots, L-1$ . The channel impulse response  $h(t, \tau)$  can be written as

$$h(t, \tau) = \sum_{\ell=0}^{L-1} c_\ell(t) \delta(t - \tau_\ell) \quad (1)$$

where  $c_\ell(t)$  is the random and time-varying fading coefficient associated with the  $\ell$ -th component arriving with time delay  $\tau_\ell$ . With symbol  $s(t)$  being transmitted, the corresponding received signal is given by

$$y(t) = s(t) \otimes h(t, \tau) + n(t) = \sum_{\ell=0}^{L-1} c_\ell(t) s(t - \tau_\ell) + n(t) \quad (2)$$

where  $n(t)$  denotes the noise at the receiver and  $\otimes$  denotes the convolutional operator. The noise at the receiver is commonly modeled as additive white Gaussian noise (AWGN) and is superimposed on the channel symbols to produce the received baseband signal  $y(t)$ . The amplitude statistics for each complex-valued fading coefficient  $c_\ell(t)$  may follow a Rician distribution if a LOS path is present, or a Rayleigh distribution in the absence of a LOS path. The Nakagami- $m$  distribution has also been used to model fading that is more or less severe than Rayleigh fading [2].

Fig. 3 shows a MIMO channel  $\mathbf{H}(t, \tau)$  with four transmit antennas and four receiver antennas, where the impulse

response  $h_{ij}(t, \tau)$  of the sub-channel between a transmitter antenna  $j$  and a receiver antenna  $i$  can be represented using a tapped delay line (TDL) model.

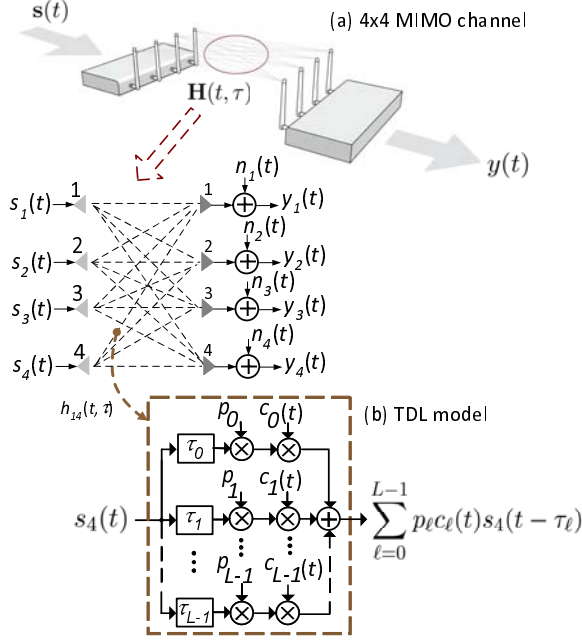


Fig. 3. (a) A 4x4 MIMO channel; (b) Tapped delay line model of the multipath fading sub-channel between transmit antenna 4 and receive antenna 1.

Due to the relatively slow changes in the radio channel, the fading coefficients  $\{c_\ell(t)\}$  are correlated in time. An important further characteristic of MIMO fading channels is the spatial correlation among the subchannels [3]. For example, the antenna-to-antenna spacing at either the TX and/or RX has a strong impact on the overall spatial correlation. Since correlations between transmit-receive antenna pairs reduce the capacity of MIMO systems, it is important that the MIMO channel emulator include a variety of parameterizable channel models that accurately describe the spatial effects and resulting channel correlations. Note that generating the fading coefficients of spatio-temporally correlated MIMO channels accurately is a computationally-daunting process.

### III. HARDWARE-BASED PHY LAYER PERFORMANCE VERIFICATION

Commercially-available BERTs [4], [5], typically include multiple general-purpose processors, digital signal processors (DSPs) and FPGAs. They create standards-compliant channel models or custom-configured models using user-defined fading parameters. Unfortunately, (i) in addition to being costly, they only support a limited number of channels, a limited number of fading paths per channel, maximum path delays, and limited bandwidths. For example, the Agilent N5106A [5] supports only  $2 \times 2$  and  $2 \times 4$  MIMO scenarios and the number of paths depends on the maximum bandwidth (e.g., 6 paths at 120 MHz, 12 paths at 80 MHz and 24 paths at 40 MHz). For scenarios requiring more than 8 sub-channels, additional units

must be synchronized to function as a single simulator, and the resulting cost is likely to be high. As another example, simulating radio channels for the 802.11ac wireless standard requires a 72-tap  $8 \times 8$  MIMO fading channel simulator with 160 MHz bandwidth, which cannot be supported with the commercially-available simulators; (ii) most commercial BERTs tend to support performance tests at the RF level. For example, baseband signals generated by the signal generator can be sent to the baseband fading channel simulator over a digital bus. The signal is faded, corrupted with AWGN, and the resulting baseband signal is sent back to a high-end RF signal generator for upconversion to RF. The modulated signal is then transmitted to the receiver DUT. The received signal is then demodulated, and the corresponding digital bit sequence is captured by a BERT. This methodology implies prolonged total setup and testing time and is the primary reason for the significant testing cost involved with commercially-available BERTs. Moreover, the analog RF section has to be prototyped and the device cannot be used at the early baseband design stage, when the costs of design changes are minimized.

It is important to decouple the verification of the baseband section from that of the RF module so that the performance of each stage can be evaluated individually. This isolates the source of potential performance problems between the baseband section and the RF front-end and, hence, degradation in performance due to various types of impairments can be more rapidly traced back to the individual modules at the RF front-end and at the signal processing blocks at the baseband section. This also minimizes system integration risk and unexpected surprises when system-level testing begins. Without RF transceivers, digital baseband simulators offer high-reproducibility tests free from RF measurement sensitivities. However, since PHY layer performance depends ultimately on the performance of both the baseband section and the RF front-end, once the performance of the baseband section and RF front-end are verified separately, it is desirable to add an RF front-end to the digital baseband simulator to fully verify all PHY layer specifications.

The primary objective of BER measurement at the RF level is to determine whether the receiver satisfies the desired BER specification. Typically, wireless standards define performance metrics in terms of the coded BER at a minimum RF input power level into the receiver. It is important to note that standards generally specify only the overall performance limits and the performance is left unspecified for the intermediate PHY layer sub-blocks. For example, when the standard specifies the BER at the output of the channel decoder, this BER performance depends on the entire PHY layer signal chain (channel propagation conditions, RF front-end, and baseband signal processing modules). The RF and baseband characteristics in their parameterized models can thus be adjusted so that the overall system-level performance requirements can be met without over-designing the RF front-end and/or baseband modules.



#### IV. FPGA-ACCELERATED DESIGN AND PERFORMANCE VERIFICATION OF DIGITAL BASEBAND COMMUNICATION SYSTEMS

Rapid prototyping has become an indispensable strategy for developing new wireless products. The fine-grained and reconfigurable architecture of FPGAs make them a flexible and efficient platform for assessing the suitability of alternative signal processing algorithms, for exploring promising architectures, and for evaluating potential performance and hardware trade-offs. FPGA-based prototyping enables the verification of PHY layer design ideas at the earliest and least expensive stage of the design process. Moreover, FPGAs now provide abundant logical resources for high-performance signal processing that make them ideal platforms for implementing new wireless technologies. Therefore, designers can effectively reuse prototyped and verified baseband signal processing modules in the implementation of the final products [6], hence reducing the overall design time. The reprogrammability of FPGAs enables engineers to track the evolution of standards as well as making the products useful across a range of applications and multi-service terminals.

An important point to note is that the partitioning of the baseband sub-blocks among different processing units has a direct impact on the overall system performance. For the purpose of simulation time acceleration, baseband signal processing algorithms with dominant computational complexity can be mapped onto an FPGA so that the major workload is transferred to the dedicated hardware. When implementing computationally-intensive and time-critical signal processing modules on an FPGA, one should also pay attention to the communication overhead and performance bottlenecks when transferring data into and out from an FPGA. With further improvements in the number of available logic resources and in the performance of FPGAs, a far better solution, which improves system throughput and reduces signal latency, is to incorporate most of the sub-blocks of the PHY layer on a single FPGA rather than over multiple devices. Therefore, to further accelerate performance verification of the baseband layer over a wide range of radio channel conditions, the digital fading channel simulator, if implemented compactly enough, can be mapped along with other baseband signal processing modules onto a single FPGA. An on-chip digital BERT simplifies test setup, alleviates the time-consuming work of calibrating external equipment, is a significantly more cost-effective solution than expensive commercially-available BERTs, and can dramatically reduce the simulation time, thereby generating results more quickly. Moreover, utilizing scalable architecture of an FPGA, the BERT ensures a simple and cost-effective upgrade to support the needs of future technologies (e.g., increasing the number of channels, multipaths and path delays).

We follow the conventional design verification methodology for the baseband section, which starts with algorithm development. Since the baseband algorithms significantly affect both the design complexity and system performance, algorithm

selection is an important decision in the baseband design. At this step, we use the high-level MATLAB and C languages, with floating-point representations of the variables, to verify the algorithms quickly in functional simulation. After validating the behavior of the algorithms, the floating-point representation of signal processing modules is converted into a suitable fixed-point representation using a comprehensive library of parameterizable fixed-point arithmetic and logical routines developed in Mex-C [7]. This library includes parameterizable modules, with adjustable bit-widths, that provide a flexible simulation environment for the bit-true comparison of approximated values with accurate function values in double precision. Minimization of the variable widths leads to more efficient hardware implementations and, hence, the hardware implementation of the baseband functionality is usually fixed-point. However, the resulting quantization errors limit the performance of the algorithm. Due to the nonlinear effects of the mapping from a floating-point to a fixed-point representation, the fixed-point design trade-offs should also be investigated with respect to quantization error and numerical stability to find the optimal word lengths and fraction lengths of all signal variables. The bitwidths of the fixed-point variables in baseband signal processing algorithms are chosen empirically based on the trade-off between the performance and area of the required hardware resources and also the level of quantization error. While the optimized floating-point models can serve as a performance reference for the fixed-point model, this step provides an initial estimate of how much precision can be safely dropped in the fixed-point design.

Fixed-point simulation of the complex signal processing algorithms, such as the channel decoder, on workstations typically requires a long time. For example, bit-level operations are often inefficient to implement on fixed word-width microarchitectures. The fine-grained and reconfigurable architecture of FPGAs is a flexible and efficient platform for implementing fixed-point signal processing algorithms with customized signal representations (i.e., with optimized word and fraction lengths). Since software-based fixed-point simulation of the entire baseband processing chain is a computationally-intensive process, in the next step, the optimized and verified fixed-point representation of the algorithms is transferred to the architectural (or register transfer) level representation using Verilog hardware description language. Hardware implementation results verified by comparing the results of post place and route simulation with bit-true fixed-point simulation results of the algorithm. At the architectural level, the design typically evolves through a succession of redesigns and optimizations to meet the design constraints, such as maximum throughput and minimum resource utilization requirements. Fortunately, as we will show, the design and verification of the baseband layer can be accelerated by several orders of magnitude using FPGA-based prototyping. Note that since components of the baseband layer frequently re-appear among different standards, designers would not typically need to develop from scratch every component of the system. They might use parameterizable off-the-shelf intellectual property (IP) blocks from various

vendors. Utilizing parameterizable IP cores not only facilitates baseband algorithm development and reducing the design time, it also enables engineers to concentrate on the wider system design optimizations.

## V. A BERT SYSTEM ON A SINGLE FPGA

To demonstrate our methodology, we developed a parameterizable hardware-based baseband BERT for multiple-antenna communication systems. To generate BER versus SNR characteristics using MC simulation, a pseudo-random number generator (PRNG) generates a sequence of uniformly-distributed random bits. The generated bit stream is then passed through various signal processing modules at the transmitter, then faded by the radio channel coefficients and corrupted further by the AWGN. A sequence of baseband signal processing modules at the receiver recovers the transmitted bits from the noisy received symbols.

It is important to note that since fading channel coefficients are correlated in time, the BER performance measurements needs to be averaged not only on independent instances of AWGN samples and transmitted bits, but also on the fading channel samples. Therefore, to accurately estimate the BER performance of a wireless communication system over a time varying fading channel, a relatively large number of random bits and noise samples are generated and the BER for every value of SNR can then be estimated based on a combination of different criteria, including the number of transmitted bits, the number of accumulated errors, and the transmission time.

Fig. 4 shows the block diagram of the implemented baseband BER performance measurement system. In the MIMO transmitter block, source bits, generated by a PRNG, are encoded using an extended binary (24, 12) Golay channel code, interleaved with a length-16383 interleaver, and modulated using 4-QAM symbols [8]. Channel coding is applied to the data bits to improve system performance and robustness in the presence of channel impairments. Typically, the fading channel response changes much slower than the data signal. Therefore, the effects of a deep fade can last over a relatively long sequence of data samples, which can result in a burst of errors. Interleaving the data samples before transmission causes bursts of errors arising in the channel to be broken up by the de-interleaver in the receiver. The resulting isolated bit errors can then be more readily detected and corrected by the error correction decoder. Then the interleaved bits are modulated and passed through the MIMO channel [9], [10] where they are attenuated by the multipath fading and corrupted with AWGN [11].

In the receiver, a maximum likelihood (ML) detector estimates the transmitted bits. After ML detection, the bit stream is de-interleaved, decoded for the extended Golay code, and compared to the transmitted bit stream. At the receiver, we used another instance of the same PRNG employed at the transmitter with the same initial seed values to generate the same sequence of random bits.

Fig. 5 shows the picture of the implemented BERT on the GVA-290 board [12] along with the power source, os-

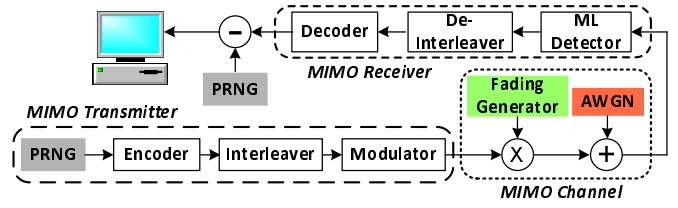


Fig. 4. Block diagram of the implemented MIMO BERT.



Fig. 5. Test setup for evaluating the baseband performance of MIMO systems on a GVA-290 FPGA board.

cilloscope, and control computer. This board contains two Xilinx Virtex-E XCV2000E FPGAs, two Xilinx Spartan-II FPGAs, four 100 Msps analog-to-digital converters, and four 100 Msps digital-to-analog converters. We implemented the entire parameterizable BERT for a  $2 \times 2$  MIMO system on only one of the Xilinx Virtex-E XCV2000E FPGAs. This FPGA includes 19200 configurable slices, 160 block memories (BRAMs) with no built-in dedicated multipliers. To be able to verify the operation of the baseband layer over different values of parameters, test automation becomes increasingly important to ensure comprehensive coverage of test scenarios. Using a custom graphical user interface (GUI) running on a host computer, the BERT can be configured for different test cases. The parameterizable BERT enables the designers to verify and optimize the transmitter and the receiver algorithms under a wide variety of system parameters. For example, the BERT can support different sample rates, modulation schemes and signal-to-noise ratios. The implemented fading channel simulator in the BERT can also be parameterized to simulate the channel characteristics of industrial standards using different power delay profiles and fading models. Currently, the BERT supports the widely-used independent and identically distributed (i.i.d) MIMO channels, where no correlation is assumed to exist between sub-channels of the MIMO system and also three of the most popular correlation-based analytical MIMO channels: the Kronecker model, the Weichselberger model, and the virtual channel representation (VCR) model [13]. The spatial correlation parameters of these three channel models, which are commonly characterized by a channel correlation matrix, are user-controllable and can be read from the BERT's GUI. The MIMO fading channel coefficients are computed dynamically on the FPGA.

TABLE I  
CHARACTERISTICS OF THE DIFFERENT MODULES ON A XILINX VIRTEX-E  
XCV2000E FPGA

Module	Slices	BRAMs	Freq. (MHz)
SRC	37 (< 1%)	—	299
Channel encoder	50 (< 1%)	—	126
Interleaver	49 (< 1%)	4 (2%)	117
Fading channel	3601 (18%)	7 (4%)	70
AWGN	634 (3%)	8 (5%)	99
ML Detector	947 (4%)	—	76
De-interleaver	50 (< 1%)	4 (2%)	115
Channel decoder	438 (2%)	—	80

On a Xilinx Virtex-E XCV2000EBG560-6 FPGA, the implemented MIMO communication system (source, encoder, interleaver, detector, de-interleaver, and decoder) utilizes less than 9% of the available configurable slices while the rest of the system (fading simulator, BER performance measurement, initialization, and interfacing modules) consumes a much larger portion of the available resources (more than 60%). Table I gives the hardware costs and performance of the implemented modules. The implemented BERT system uses 13436 (69%) of the slices and 47 (29%) of the BRAMs of the FPGA, and operates at 52 MHz. With one Virtex-E FPGA dedicated to the fading channel simulator and interfacing modules, the other on-board FPGAs can be utilized to prototype yet more complex wireless communication systems.

Fig. 6 shows the measured BER performance of the implemented coded  $2 \times 2$  MIMO system over various radio channel conditions. In this platform, the sample rate is set to 3.125 Msps or 12.5 Mbps (the maximum speed supported by the ML detector), and the Doppler frequency is 350 Hz. The channel state information is assumed to be available at the receiver, hence no channel estimation was performed. To ensure statistically-meaningful BER measurements over a time-varying channel, the measurements need to be averaged over time for a sufficient number of generated samples. To estimate each BER point at each SNR, we measured the performance over at least 1023 seconds of signal transmission on the hardware platform, and when at least 100 errors were found at the Golay decoder output. Note that the BER performance of a wireless communication system can vary significantly under various radio channel models, as shown in Fig. 6. Therefore, employing faithful radio channel models is very important for accurate performance measurement.

It is important to note that:

- The BERT modules were developed using device-independent HDL and no specific features of the FPGAs, such as built-in soft processors, were utilized. Therefore, the system is portable and can be easily synthesized onto larger and faster new FPGAs for the rapid prototyping of increasingly complex emerging wireless communication systems.
- The baseband layer of different communication systems could have different numbers and types of signal processing modules. The flexible layered architecture of our BERT could easily cascade a variety of signal processing modules, each operating at a possibly different rate. Using our simulator we

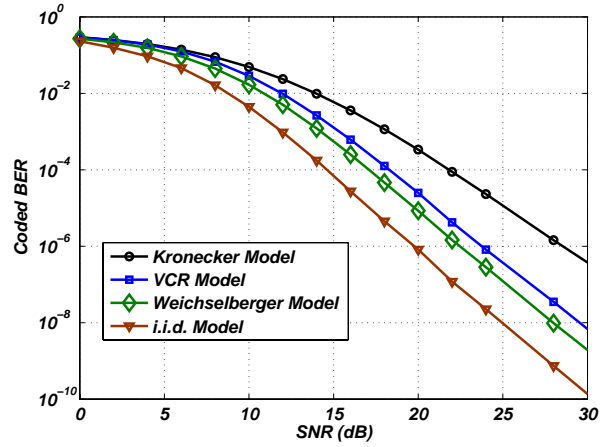


Fig. 6. Measured BER performance of a  $2 \times 2$  MIMO system over different channel models.

can compare different signal processing algorithms to quantify the BER performance versus system resource trade-offs. In addition, the fading channel simulator is readily scalable to support MIMO systems with arbitrary numbers of transmitter and receiver antennas.

- Despite the numbers and types of signal processing modules employed at the baseband section of different wireless communication standards, a faithful fading channel simulator and an accurate AWGN generator are two fundamental components for the baseband performance measurement of wireless systems. Our BERT utilizes the most compact with the highest throughput digital baseband fading channel simulator from [9], [10]. For example, on a Xilinx Virtex-4 LX200 FPGA, up to 1184 different paths can be implemented simultaneously, while generating  $1184 \times 342$  million  $2 \times 16$ -bit complex-valued fading samples per second. These independent streams of fading samples, while they cannot be provided by costly commercially-available channel emulators, can be configured to simulate various wireless communication systems, including wireless networks with a relatively large number of nodes and with the option of multiple antennas per node. Also, we utilized the ultra-compact AWGN module from [11], which generates accurate Gaussian samples to the tails of the distribution required for low BER measurements.

- Even though software development of fixed-point baseband signal processing modules is faster than hardware design and implementation of the BERT, accurate performance measurement of complex baseband sections in emerging standards using a bit-true model on time-varying channels is a computationally-daunting process. For example, 10 seconds of BER measurements using our hardware platform take more than three days of bit-true software simulation in C running on a 3.6-GHz dual-core Pentium processor with 1 GB of RAM. This corresponds to a speed-up of over 25,000. Simulation times vary significantly and depends on various factors, such as the the number of antennas (single or multiple antennae), the types of antennas (directional or omnidirectional), the number of taps and the spatio-temporal correlation properties

of the fading channels, the complexity of the baseband signal processing algorithms (e.g., modulation order, error control codes, detection algorithms, etc.). For example a geometric fading channel is significantly more complex than a simple Rayleigh fading channel widely used for software-based simulations. Also, using stronger error control codes and more accurate detection algorithms impact the bit-true simulation time significantly.

It is important to note that the example speed-up is for the performance verification of the baseband sections under one test configuration. However, a relatively large number of operating modes and test configurations must be verified for the baseband algorithms of multiple antenna systems. Therefore, despite the longer development time of baseband layer in hardware, bit-true performance verification of complex signal processing algorithms under various operating modes and test configurations using an FPGA-based BERT is significantly faster than software-based verification. Therefore, the single-FPGA BERT can significantly accelerate the overall performance verification of baseband sections. Nevertheless, designers might use off-the-shelf intellectual property (IP) blocks from various vendors. Utilizing parameterizable IP cores not only facilitates baseband algorithm development and reducing the design time, it also enables engineers to concentrate on the wider system design optimizations. Nevertheless, designers might use off-the-shelf intellectual property (IP) blocks to facilitate system development, to reduce the design time, and to enable engineers to concentrate on the broader system design optimizations.

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