

An Accurate MIMO Fading Channel Simulator Using a Compact and High-Throughput Reconfigurable Architecture

Amirhossein Alimohammad, Saeed Fouladi Fard
Ukalta Engineering, 4344 Enterprise Square
10230 Jasper Ave, Edmonton, AB, T5J 4P6, Canada
Email: {amir, saeed}@ukalta.com

Bruce F. Cockburn
Department of Electrical and Computer Engineering
University of Alberta, Edmonton, AB, T6G 2V4, Canada
Email: cockburn@ualberta.ca

Abstract—This article presents an ultra-compact and high-throughput reconfigurable architecture for implementing an efficient fading channel simulator that supports a relatively large number of propagation paths. To closely reflect actual radio signal propagation conditions, we used a recently improved Rayleigh and Ricean fading channel model based on the sum-of-sinusoids technique. The improved model is optimized for a significantly more compact hardware implementation. To achieve a fast fading variate generation rate with much less hardware and no significant loss in accuracy, instead of generating fading samples directly, the new scheme first generates fading samples at a lower rate using a time-multiplexed datapath that can be fit into a small fraction of a field-programmable gate array (FPGA). In the second step, the simulator uses a compact multiplication-free linear interpolator to produce the fading samples between variates generated at a lower rate. Implementing a 64-path fading channel simulator on a Xilinx Virtex-4 XC4VLX200-11 FPGA requires only 13044 (14%) of the configurable slices, 10 (2%) of the block memories, and one (1%) of the dedicated DSP blocks, while generating 64×191 million complex-valued fading samples per second. The simulated paths can be readily combined to form high path count models for multiple-input multiple-output systems as well as frequency-selective channels.

Index Terms—Rayleigh fading, Ricean fading, sum-of-sinusoids model, hardware-accelerated simulation, MIMO channel model.

I. INTRODUCTION

Emerging wireless communication standards provide higher data rates, more efficient spectrum utilization and improved user services. Multiple-input multiple-output (MIMO) wireless communication technology has been included in many recent wireless standards, such as IEEE 802.11 *n*, 802.16 *m* and 802.20, to increase both the data rate and spectrum efficiency over traditional single-antenna transmission. To keep up with the fast evolution of communication technologies and wireless standards, the design verification and characterization environment must be configurable to provide reliable and repeatable measurements. Unfortunately, the high computational complexity of the conventional fixed-point software simulation of MIMO communication systems makes software simulations increasingly impractical for the performance evaluation of high-throughput broadband systems. Fortunately, hardware-accelerated prototyping of both the design and test environ-

ment now offers the potential to significantly shorten the design cycle and reduce the time-to-market.

Field-programmable gate array (FPGA) technology has already been adopted to speed up the prototyping and verification of new communication systems [1], [2]. Ideally, the full communication system chain (i.e., the transmitter, fading channel simulator and the receiver) should be prototyped completely in a single device. A parameterizable and accurate fading channel simulator is a crucial component for the repeatable baseband design and verification of wireless communication systems. Commercially-available fading channel simulators (e.g., [3]–[5]) are stand-alone units that are relatively costly and cannot be miniaturized to fit onto a single device along with the rest of the prototyped system. A single-chip characterization system avoids the need for external interfaces that connect bulky and expensive test equipment to the device under test. In addition, while commercial testers support only a limited number of channels, these testers cannot be readily scaled-up for simulating scenarios where the number of simultaneous communication channels is large, such as when ad-hoc networks and MIMO channels with a relatively large number of antennas to be simulated.

One well-known technique for simulating fading channels is the filter-based method [6]. In this approach, to generate the in-phase and quadrature components of fading variates with the required correlation between variates, two independent, zero-mean, white Gaussian random variables with identical variance are passed through a low-pass filter. This filter is often called the shaping filter for it determines the power spectrum shape and the temporal correlation function of the fading process. Unfortunately, this technique has relatively high computational complexity and is inconvenient for implementing a large number of fading channels on a single FPGA [7]. For an especially compact hardware implementation that supports a large number of propagation paths, we utilize the so-called sum-of-sinusoids (SOS) technique [8]. In this approach the fading process is modeled by superimposing a sufficient number of sinusoidal waveforms with amplitudes, frequencies and phases that are selected appropriately to generate the desired statistical properties. The SOS-based technique is

widely used in the COST 259, COST 273, and IST-Winner fading channel models [9], [10].

Various computationally-efficient fading channel models have been proposed over the last three decades that involve superimposing an acceptably small number of sinusoids. Since the performance of communication systems strongly depends on time-varying fading channel characteristics, it is crucial to choose a channel model that faithfully reproduces the statistical properties of the actual propagation conditions. Even though some of the already proposed fading models utilize only a small number of sinusoids and, hence, are computationally-efficient, their statistical accuracy has been questioned [11]–[14]. Despite the known limitations in the statistical properties of most existing SOS-based models, several compact fading channel simulators that can be implemented on a small fraction of a single FPGA have been described in the literature [14]–[24]. However, these hardware implementations are still not compact enough to permit a large number of paths to be implemented on a single FPGA.

In this article we propose an efficient reconfigurable architecture for implementing a relatively large number of independent streams of fading samples that can be parameterized separately to simulate different propagation conditions. The new architecture is compact enough to allow various fading scenarios (e.g., single and multipath, Rayleigh and Ricean fading channels for single and multiple antenna communication) to be simulated on a single FPGA. To implement this architecture, first we chose the recently improved SOS-based fading channel model from [14] that can generate a sequence of fading samples with accurate statistics. We propose a new update procedure for the sinusoid parameters of the SOS-based fading channel model. This optimization results in a significantly more compact hardware implementation of Rayleigh and Ricean fading channels with a relatively large number of paths. As opposed to the design in [14], which generates fading samples directly, the new fading channel simulator supports higher throughput and generates fading variates in two consecutive stages. First the fading sequence is generated at a much slower rate. This allows us to utilize a compact time-multiplexed architecture to generate correlated fading variates. Then we use a multiplication-free linear interpolator to produce fading samples at the desired higher sample rate. An important property of the proposed architecture is that since the same datapath is shared to generate fading variates at a lower rate, the number of superimposed sinusoids mainly impacts the size of the memories used to store the sinusoid parameters and thus has almost no impact on the computational complexity of the proposed fading channel simulator.

The rest of this article is organized as follows. Section II reviews related work on Rayleigh fading channel models and compares the important statistical properties of three well-known SOS-based models. Section III presents our modifications that allow for a more efficient hardware implementation. In Section IV we describe our compact and high-throughput reconfigurable architecture for a single-FPGA implementation of the fading channel simulator with a large number of inde-

pendent channels. Finally, Section V makes some concluding remarks.

II. RELATED WORK ON RAYLEIGH FADING MODELS

A fading channel is commonly modeled as a complex Gaussian wide-sense stationary (WSS) uncorrelated scattering process $c(t) = c_i(t) + jc_q(t)$ over time t , where the envelope $|c(t)|$ follows the Rayleigh distribution [8]. In a two-dimensional isotropic scattering environment with an omnidirectional receiving antenna at the receiver, the autocorrelation function (ACF) associated with either $c_i(t)$ or $c_q(t)$ is ideally $R_{c_i, c_i}(\tau) = R_{c_q, c_q}(\tau) = \mathcal{J}_0(2\pi f_D \tau)$, where f_D is the maximum Doppler frequency and $\mathcal{J}_0(\cdot)$ is the zeroth-order Bessel function of the first kind. The cross-correlation function (CCF) between $c_i(t)$ and $c_q(t)$ is ideally $R_{c_i, c_q}(\tau) = R_{c_q, c_i}(\tau) = 0$.

In general, SOS-based models can be classified as either deterministic and stochastic models. Deterministic models use constant parameters (gains, frequencies and phases) while the parameters in stochastic models (e.g., gains and/or frequencies) are random variables. Over the past three decades, many deterministic and stochastic SOS-based fading channel models have been proposed. However, only a few have shown improved statistical properties over earlier models to the extent that they have become accepted as new benchmarks [13]. Several important characteristics should be considered when choosing a SOS-based model for simulating fading channels. These properties are discussed below using four widely-used fading models.

The Rayleigh fading model of Li *et al.* [25] (henceforth called *Model I*) can be written in discrete time as follows:

Model I:

$$c_i[m] = \sqrt{\frac{1}{N}} \sum_{n=0}^{N-1} \cos(2\pi f_D T_s m \cos \alpha_n + \varphi_n)$$

$$c_q[m] = \sqrt{\frac{1}{N}} \sum_{n=0}^{N-1} \sin(2\pi f_D T_s m \sin \alpha_n + \psi_n)$$

where N is some sufficiently large number of sinusoids, m is the discrete-time index, $f_D T_s$ is the normalized maximum Doppler frequency, T_s is the sample period, and $\alpha_n = 2\pi n/(4N) + \alpha_o$ is the angle of arrival of the n -th sinusoid where $0 < \alpha_o < 2\pi/N$ and $\alpha_o \neq \pi/N$. The phase parameters of the n -th sinusoidal components, φ_n and ψ_n , are statistically independent and uniformly-distributed random variables over $[-\pi, \pi)$, for all n .

In the deterministic *Model I*, since the values of the parameters are constants, only one simulation trial is sufficient to represent the statistical properties of the generated fading sequence. Fig. 1 shows the ACF of the quadrature component and the CCF between quadrature components $c_i(t)$ and $c_q(t)$. While the ACF approaches the reference function by increasing the number of sinusoids, the CCF deviates from the reference value, as shown in Fig. 1, even for greater values of N . Unfortunately, this property is common among many other

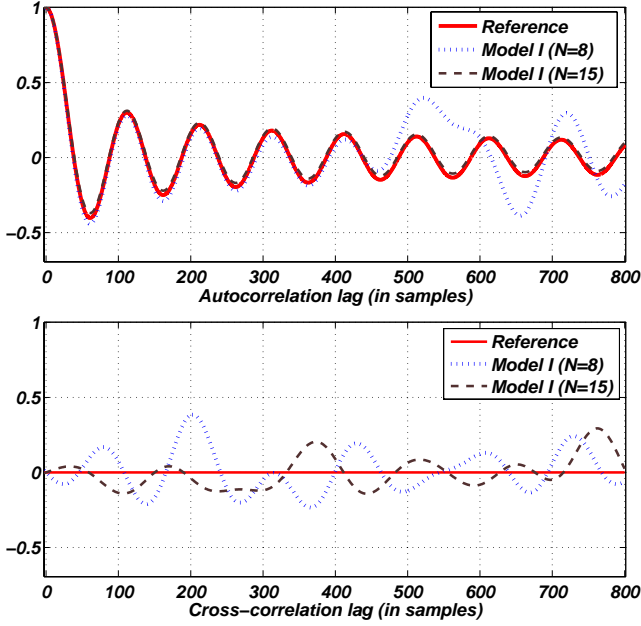


Fig. 1. ACF and CCF of *Model I* for one block containing 10^5 fading samples with $f_D T_s = 0.01$.

proposed deterministic models, such as [25]–[28], as the CCF deviates from the reference function [29].

The deterministic model recently proposed by Pätzold *et al.* [29] (henceforth called *Model II*) can be written in discrete time as follows:

Model II:

$$c_i[m] = \frac{2}{\sqrt{N}} \sum_{n=1}^N \cos(2\pi f_n T_s m + \varphi_n)$$

$$c_q[m] = \frac{2}{\sqrt{N}} \sum_{n=1}^N \cos(2\pi \dot{f}_n T_s m + \psi_n)$$

where φ_n and ψ_n are statistically-independent and uniformly-distributed random variables over $[0, 2\pi)$, for all n , and the discrete Doppler frequencies f_n and \dot{f}_n of the n -th sinusoid are defined as

$$f_n = f_D \cos\left(\frac{\pi(3n-1)}{6N}\right),$$

$$\dot{f}_n = f_D \cos\left(\frac{\pi(3n-2)}{6N}\right).$$

As shown in Fig. 2, the CCF between the quadrature components of the generated fading sequence approaches more closely to the theoretical reference value of zero compared to *Model I*. *Model II* has lower computational complexity and better statistical properties compared to *Model I* (and most earlier deterministic models); nevertheless, as shown in [29], the statistical properties of generated fading sequence deviate from the reference values at large lags, which might not be acceptable for some communication systems.

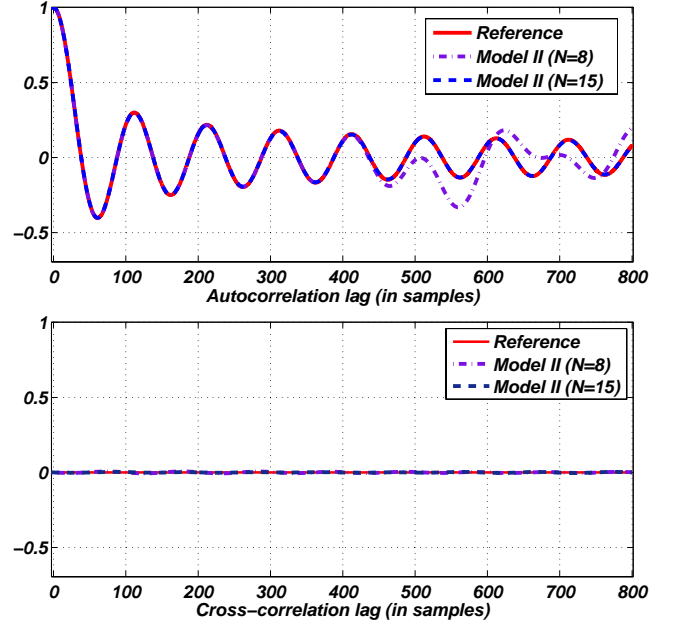


Fig. 2. ACF and CCF of *Model II* for one block containing 10^5 fading samples with $f_D T_s = 0.01$.

The stochastic Rayleigh model proposed by Zajić *et al.* [30] (henceforth called *Model III*) can be written in discrete time as follows:

Model III:

$$c_i[m] = \frac{1}{\sqrt{N}} \sum_{n=1}^N 2 \cos(\beta_n) \cos(2\pi f_D T_s m \cos \alpha_n + \varphi_n)$$

$$c_q[m] = \frac{1}{\sqrt{N}} \sum_{n=1}^N 2 \sin(\beta_n) \sin(2\pi f_D T_s m \cos \alpha_n + \varphi_n)$$

where $\alpha_n = (2\pi n - \pi + \theta)/(4N)$ and φ_n , β_n and θ are statistically-independent and uniformly-distributed random variables over $[-\pi, \pi)$, for all n .

An important first point to note is that the computational requirements of SOS-based models can vary significantly. For example, *Model III* is more computationally complex than *Model I* and *Model II* as it requires summing the products of trigonometric functions. To highlight this additional complexity, one can use identities to rewrite *Model III* as:

$$c_i[m] = \frac{1}{\sqrt{N}} \sum_{n=1}^N \cos(2\pi f_D T_s m \cos \alpha_n + \varphi_n + \beta_n)$$

$$+ \frac{1}{\sqrt{N}} \sum_{n=1}^N \cos(2\pi f_D T_s m \cos \alpha_n + \varphi_n - \beta_n)$$

$$c_q[m] = \frac{1}{\sqrt{N}} \sum_{n=1}^N \cos(2\pi f_D T_s m \cos \alpha_n + \varphi_n - \beta_n)$$

$$- \frac{1}{\sqrt{N}} \sum_{n=1}^N \cos(2\pi f_D T_s m \cos \alpha_n + \varphi_n + \beta_n)$$

We can see that *Model III* uses twice as many sinusoids as *Model I* and *Model II*. Therefore, to ensure fair comparisons of their statistical properties, one should halve the value of N for *Model III* with respect to the N value used in *Models I* and *II*.

The second important point to note is that the parameters of the stochastic models are random variables and the statistical properties of every simulation trial changes. When the statistical properties of generated fading samples are averaged over only one block of fading samples, they do not converge to the reference properties. Fig. 3 shows that the ACF of the quadrature component for one block containing 10^5 fading samples with $f_D T_s = 0.01$ deviates significantly from the reference function.

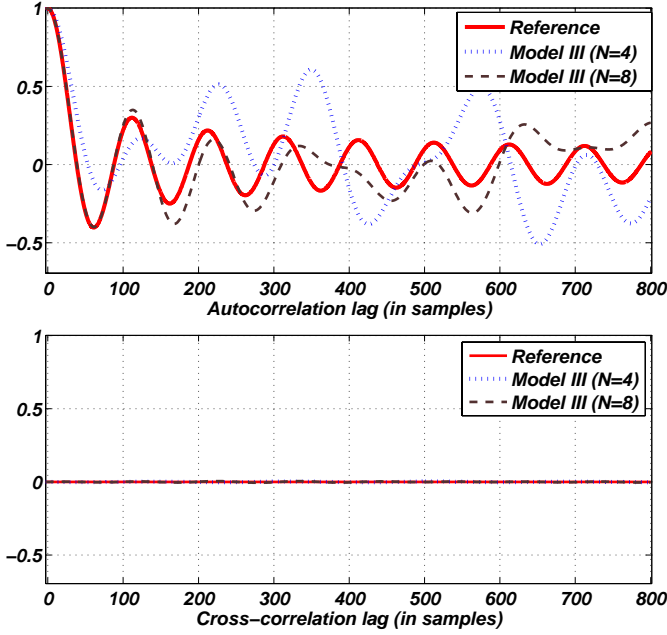


Fig. 3. ACF and CCF of *Model III* for one block containing 10^5 fading samples with $f_D T_s = 0.01$.

While this model, and in general most earlier stochastic models such as [31]–[33], have inaccuracies with respect to matching the reference ACF over every simulation trial, their statistical properties converge to the desired properties only by averaging over a sufficiently large number of generated blocks. Fig. 4 shows that the ACF and CCF properties of generated fading variates are relatively close to the reference values, especially for $N = 8$ sinusoids.

Since ensemble averaging greatly improves the statistical properties of stochastic SOS-based models, these models can be used to simulate block-based wireless systems, where the channel can be assumed to change randomly between two consecutive blocks (e.g., in the burst error analysis of mobile communication systems). However, the increased statistical accuracy from ensemble averaging comes at the cost of significantly increased computation and, hence, longer simulation times and greater simulator implementation cost. In addition, generating a new set of parameters at the beginning of every

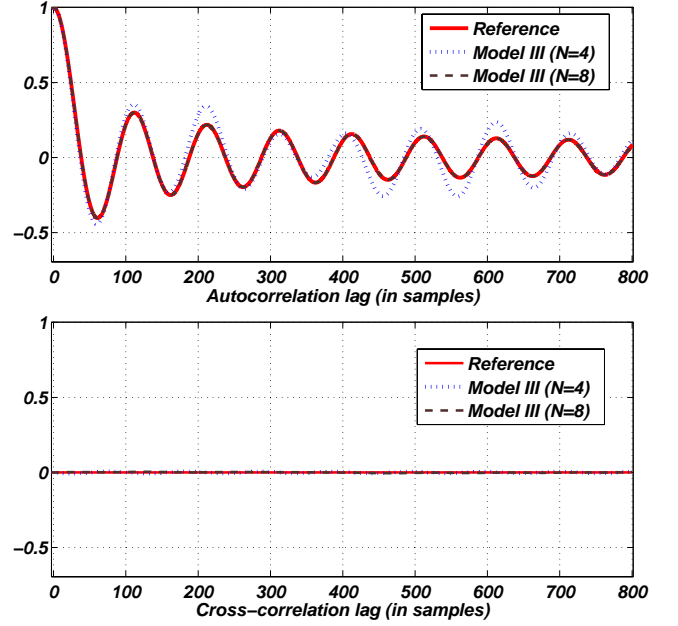


Fig. 4. ACF and CCF of *Model III* for 30 blocks containing 10^5 fading samples with $f_D T_s = 0.01$.

transmitted block is an inconvenience in the simulation of continuous communication.

When implementing a fading channel simulator for a practical communication system, it is preferable to have the lowest possible complexity algorithm that generates a fading process $c(t)$ whose statistical properties match those of the reference model over every transmitted block of any arbitrary length. An accurate SOS-based fading channel model (henceforth called *Model IV*) that (a) is stochastic; (b) ensures that the statistical properties of every generated block closely match those of the reference model; and (c) requires only a small number of sinusoids with a low computational complexity, was proposed in [14]. This improved SOS-based model can be written in discrete time as follows:

Model IV:

$$c_i[m] = \frac{1}{\sqrt{K+1}} \left[\sqrt{K} \cos(2\pi f_D T_s m \cos \theta_o + \phi_o) + \sqrt{\frac{1}{N}} \sum_{n=1}^N \cos(2\pi f_D T_s m \cos \alpha_n[m] + \varphi_n[m]) \right] \quad (1)$$

$$c_q[m] = \frac{1}{\sqrt{K+1}} \left[\sqrt{K} \sin(2\pi f_D T_s m \cos \theta_o + \phi_o) + \sqrt{\frac{1}{N}} \sum_{n=1}^N \cos(2\pi f_D T_s m \sin \alpha_n[m] + \psi_n[m]) \right], \quad (2)$$

where K is the Ricean factor and the line-of-sight (LOS) component is modeled as a zero-mean stochastic sinusoid with a fixed angle of arrival θ_o and initial phase ϕ_o that are uniformly distributed random variables over $[-\pi, \pi)$. The Rayleigh component of *Model IV* uses independent random

walk processes (RWPs) [34] for the $2N + 1$ sinusoid parameters θ , φ_n and ψ_n instead of random variables, as used in *Models I* and *II*. The angle of arrival of the n -th path is updated according to the RWP $\theta[m]$ in the expression $\alpha_n[m] = (2\pi n - \pi + \theta[m])/(4N)$. It is shown in [14] that the key statistical properties of the generated fading samples—such as autocorrelation, cross-correlation, and level crossing rate—produced by *Model IV* do indeed closely match the ideal statistics, even when summing only $N = 8$ sinusoids. Therefore, we use *Model IV* as the most accurate available reduced complexity SOS-based model for implementing the new fading channel simulator.

III. MODIFICATION OF THE ACCURATE SOS-BASED FADING CHANNEL MODEL FOR EFFICIENT HARDWARE SIMULATOR IMPLEMENTATION

We modified the update procedure for the RWPs presented in [14] to achieve a significantly more compact hardware implementation of a high-path count fading channel simulator. Algorithm 1 describes our new procedure for updating the $2N + 1$ RWPs θ , $\varphi_n[m]$ and $\psi_n[m]$, where m is the fading sample index and the “fadingLength” is the block length of the generated fading samples.

Each RWP is initialized with a uniformly-distributed random value between $[-\pi, \pi)$ and an initial walking direction $s = 1$. The RWP updates between $[-\pi, \pi)$ with a very small signed step size δ towards π when $s = 1$, while a direction of $s = -1$ updates towards $-\pi$. When the absolute value of the RWP exceeds π , then the update direction is reversed. For suitably slowly changing RWPs θ , φ_n and ψ_n , the unsigned coefficient ξ is chosen to be small enough that the step size δ produces highly correlated angles of arrival and path phases. The very small signed values of δ are generated by multiplying the very small constant ξ by a generated random variable $u[m]$, which is a source of independent, uniformly-distributed samples over $[0, 1)$. Using numerical simulations we will show that updating the RWPs only every few clock cycles (instead of updating them in every clock cycle, as was used in [14]) has negligible impact on the statistical properties of the fading process. In this case, we can utilize a shared hardware datapath to update all $2N + 1$ RWPs, which minimizes the resource requirements. To update the RWPs only every η clock cycles, ξ (which depends on the normalized Doppler rate) must be chosen appropriately. Some suitable predefined values of ξ for various normalized Doppler rates were suggested in [14]. The coefficient $\sqrt{\eta}$ in the step size parameter δ compensates for the skipped update cycles. To further simplify the hardware that updates the RWPs, we used the nearest power-of-2 to $\lceil \log_2(\sqrt{\eta}\xi) \rceil$ to avoid multiplications in δ_χ .

To verify the accuracy of *Model IV* using our modified update procedure for the sinusoid parameters, we compared fixed-point simulation results of the key statistical properties of the generated fading variates (using $N = 8$ sinusoids) with the reference functions. We present results for two Ricean factors: $K = 0$ (Rayleigh) and $K = 3$. As shown in Fig. 5, the autocorrelation of the real part of the complex envelope

Algorithm 1 Update procedure for RWPs θ , φ_n and ψ_n .

```

1: //Initializing RWPs
2:  $\theta[0] = \text{U}[-\pi, \pi]$ ;
3:  $s_\theta = 1$ ; // Initial updating direction
4: for  $n = 1 : N$  do
5:    $\varphi_n[0] = \text{U}[-\pi, \pi]$ ;  $s_{\varphi[n]} = 1$ ;
6:    $\psi_n[0] = \text{U}[-\pi, \pi]$ ;  $s_{\psi[n]} = 1$ ;
7: end for
8: Initialize  $\xi \ll 1$ ; // Unsigned small constant
9: // Updating RWPs
10: for  $m = 1 : \text{fadingLength}$  do
11:   if  $\text{mod}(m, \eta) == 0$  then
12:     // Update RWPs only every  $\eta$  clock cycles
13:      $\delta_\theta = s_\theta \times \xi \times u[m] \times \sqrt{\eta}$ ; // Signed updating step size
14:     // Updating  $\theta[m]$ 
15:      $\theta[m] = \theta[m-1] + \delta_\theta$ ;
16:     if  $\theta[m] \geq \pi$  then
17:        $\theta[m] = \pi$ ;
18:        $s_\theta = -s_\theta$ ; // Updating towards  $-\pi$ 
19:     end if
20:     if  $\theta[m] < -\pi$  then
21:        $\theta[m] = -\pi$ ;
22:        $s_\theta = -s_\theta$ ; // Updating towards  $+\pi$ 
23:     end if
24:     // Updating  $2N$  RWPs  $\varphi_n[m]$  and  $\psi_n[m]$ 
25:     for  $\chi_n \in \{\varphi_n, \psi_n\}$  do
26:       for  $n = 1 : N$  do
27:          $\delta_{\chi_n} = s_{\chi_n} \times \xi \times u[m] \times \sqrt{\eta}$ ; // Signed updating step size
28:          $\chi_n[m] = \chi_n[m-1] + \delta_{\chi_n}$ ;
29:         if  $\chi_n[m] \geq \pi$  then
30:            $\chi_n[m] = \pi$ ;
31:            $s_{\chi_n} = -s_{\chi_n}$ ; // Updating towards  $-\pi$ 
32:         end if
33:         if  $\chi_n[m] < -\pi$  then
34:            $\chi_n[m] = -\pi$ ;
35:            $s_{\chi_n} = -s_{\chi_n}$ ; // Updating towards  $+\pi$ 
36:         end if
37:       end for
38:     end for
39:   end if
40: end for

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$c(t)$ for one block containing 2×10^6 fading samples, with $f_D T_s = 0.01$ and $\theta_o = \pi/4$, overlies the reference functions for both the Rayleigh and Ricean fading cases computed using double-precision floating-point arithmetic. For Ricean fading, the reference ACFs and CCFs of the quadrature components are given by the following equations [35]:

$$\begin{aligned}
\text{R}_{c_i, c_i}(\tau) &= \text{R}_{c_q, c_q}(\tau) = [\mathcal{I}_0(2\pi f_D \tau) \\
&\quad + K \cos(2\pi f_D \tau \cos \theta_o)] / (2 + 2K) \\
\text{R}_{c_i, c_q}(\tau) &= -\text{R}_{c_q, c_i}(\tau) = K \sin(2\pi f_D \tau \cos \theta_o) / (2 + 2K)
\end{aligned}$$

Comparing Fig. 3 with Fig. 5 shows that utilizing RWPs instead of random variables for the parameters of the sinusoids significantly improves the time-averaged statistical properties of the generated fading samples. The increased accuracy is achieved with a relatively small number of sinusoids (e.g., $N = 8$) and without requiring ensemble averaging. Fig. 6

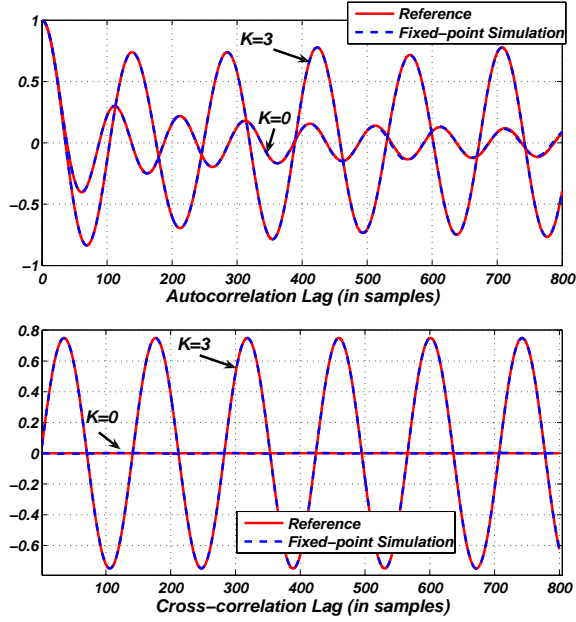


Fig. 5. ACF and CCF of the real part of the complex envelope $c(t)$ for one block containing 2×10^6 fading samples for $K = 0$ (Rayleigh), 1 and 3.

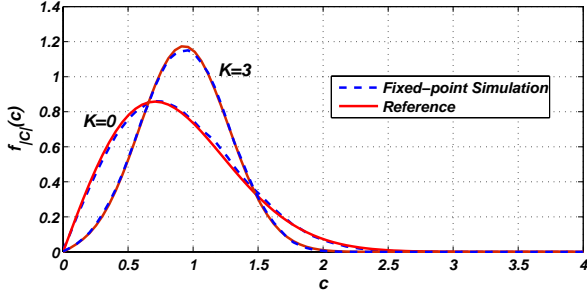


Fig. 6. PDF of the fading envelope $|c(t)|$.

shows excellent agreement for the probability density function (PDF) of the fading envelope between the simulated results and the reference functions. The theoretical PDF of the fading envelope is given by [35]:

$$f_{|C|}(c) = 2(1+K)z \cdot \exp[-K - (1-K)z^2] \cdot \mathcal{I}_0\left[2z\sqrt{K(1+K)}\right], \quad z \geq 0$$

where $\mathcal{I}_0(\cdot)$ is the zeroth-order modified Bessel function of the first kind [36]. The resulting close agreement between the simulated and reference LCRs for both Rayleigh and Ricean fading is shown in Fig. 7. The reference LCR of the fading envelope is given by [35]:

$$L_{|C|} = \sqrt{\frac{2(1+K)}{\pi}} \lambda f_D \cdot \exp[-K - (1+K)\lambda^2] \cdot \int_0^\pi \left[1 + \frac{2}{\lambda} \sqrt{\frac{K}{K+1}} \cos^2 \theta_o \cdot \cos \alpha\right] \cdot \exp[2\lambda \sqrt{K(1+K)} \cos \alpha - 2K \cos^2 \theta_o \cdot \sin^2 \alpha] d\alpha.$$

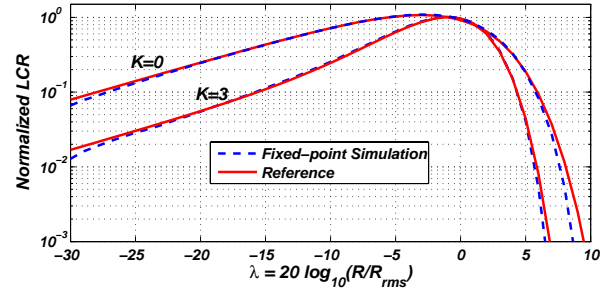


Fig. 7. Normalized LCR for one block containing 2×10^6 fading samples with $f_D T_s = 0.01$ and $N = 8$.

Figures 5-7 confirm that the modified updating procedure for the parameters of the sinusoids has negligible impact on the important statistical properties of generated fading variates.

IV. COMPACT AND HIGH-THROUGHPUT HARDWARE IMPLEMENTATION

In typical scenarios, the Doppler frequency f_D is significantly smaller than the signal sampling rate $F_s = 1/T_s$. Since the channel changes only slowly compared to F_s , the fading channel simulator can update at a much lower sampling rate. Therefore we propose a time-multiplexed scheme to implement a compact fading channel simulator. In this approach, we use shared functional and storage resources to update the RWPs and also to generate the fading process $c[m]$, resulting in a significantly smaller hardware implementation compared to previous simulators [14]–[24].

When compactness is achieved through time-multiplexing, the raw fading sample generation rate will be reduced proportionally. To compensate for this reduction, we utilize a linear interpolator to achieve the desired output sample rate. For accurate linear interpolation, the signal bandwidth should be small enough that the interpolator response does not significantly impact the statistics of the generated samples. More specifically, if the initial sample rate $\hat{F}_s \geq 64 \times f_D$ is used, a linear interpolator attenuates the image signals by more than 80 dB with no significant effect on the desired signal.

Fig. 8 shows the datapath for generating the in-phase component of the fading process, where the signals are represented in the 2's complement fixed-point format $Q(WL, WF)$, i.e., WL -bit words with a WF -bit fraction. For a clearer presentation, we describe the proposed channel simulator datapath using three processing steps:

(1) Updating the RWPs θ , φ_n and ψ_n : We define $\hat{\alpha}_n[m] = \alpha_n[m]/(2\pi) = (n - \hat{\theta})/(4N)$, where $\hat{\theta} \in [0, 1)$ and thus $\hat{\alpha}_n[m] \in [0, 1/4)$. We also define $\hat{\varphi}_n[m] = (\pi + \varphi_n[m])/(2\pi)$ and $\hat{\psi}_n[m] = (\pi + \psi_n[m])/(2\pi)$ to be in the range $[0, 1)$. Note that adding π to the random phases does not change their statistical properties. Correspondingly, when implementing Algorithm 1 we changed $\chi \in U(-\pi, \pi)$ to be $\chi \in U(0, 1)$. The pseudo-random number generator (PNG) in Fig. 8 generates uniformly-distributed samples in $Q(16, 15)$ format. The common size of on-chip memories RAM_α , RAM_φ

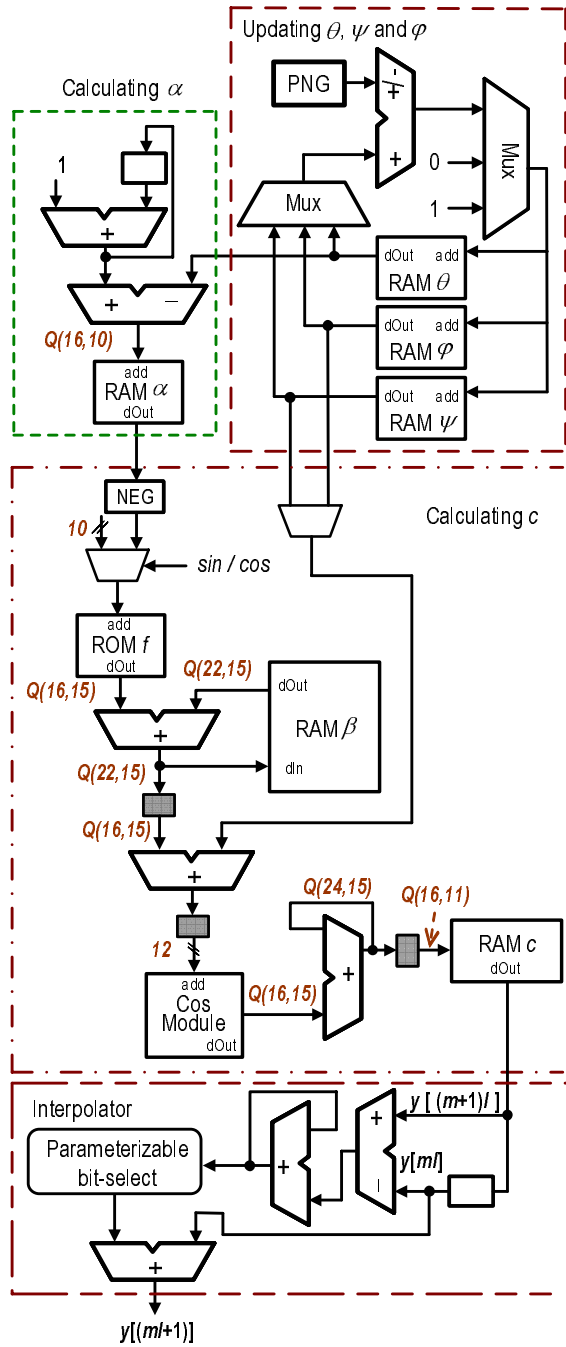


Fig. 8. Datapath for generating the in-phase component of the fading process.

φ , and $RAM \psi$ is $L \times N \times 16$, where L is the number of independent paths and each 16-bit sinusoid parameter is stored in 2's complement format $Q(16, 15)$. For example, utilizing the 18-Kb on-chip block memories on available Xilinx FPGAs [37], each one of the parameters $\hat{\alpha}_n, \hat{\varphi}_n, \hat{\psi}_n$ for $L = 32$ different simulated paths with $N = 32$ can be stored in one block memory (BRAM), as shown in Fig 8. L different values of $\hat{\theta}$ are also stored in a dual-port $RAM \theta$.

(2) Generating the Rayleigh fading process at a low rate: Based on the discrete-time definitions in (1) and (2), which

operate at a sample rate F_s , we define $\hat{c}_i[m]$ operating at a reduced sample rate $\hat{F}_s (< F_s)$ as follows:

$$\hat{c}_i[m] = \sqrt{\frac{2}{N}} \sum_{n=1}^N g(f(\frac{1}{4} - \hat{\alpha}_n[m]) \frac{m}{64} + \hat{\varphi}_n[m]) \quad (3)$$

where $g(x) = \cos(2\pi x)$ and $f(x) = 64 \times (f_D / \hat{F}_s) \sin(2\pi x)$ for $x \in [0, 1/4)$. Since we chose $\hat{F}_s \geq 64 \times f_D$, the value of $f(x)$ is limited to the range $[0, 1]$. As shown in Fig. 8, the values of $f(x)$, for $x \in [0, 0.25)$, are precomputed by uniformly quantizing the domain into 1024 segments and then storing the function values in ROM f . Note that the inner sine function in (3) is obtained using the identity $\cos(2\pi x) = \sin(2\pi(1/4 - x))$. For $x \in [0, 1/4)$, $1/4 - x$ can be calculated using the negation NEG operation. The multiplication of m and $f(\cdot)$ in (3) can be replaced with a running sum as follows:

$$f(\frac{1}{4} - \hat{\alpha}_n[m])m \approx \beta_{in}[m] = \sum_{j=1}^m f(\frac{1}{4} - \hat{\alpha}_n[j]). \quad (4)$$

Note that $\beta_{in}[m]$ can be written in recursive form as $\beta_{in}[m] = \beta_{in}[m-1] + f(1/4 - \hat{\alpha}_n[m])$ with $\beta_{in}[-1] = 0$. With similar modifications to $\hat{c}_q[m]$, the resulting simplified in-phase and quadrature components can be written in discrete-time as:

$$\hat{c}_i[m] \approx \sqrt{\frac{2}{N}} \sum_{n=1}^N g(\beta_{in}[m]/64 + \hat{\varphi}_n[m]), \quad (5)$$

$$\hat{c}_q[m] \approx \sqrt{\frac{2}{N}} \sum_{n=1}^N g(\beta_{qn}[m]/64 + \hat{\psi}_n[m]), \quad (6)$$

where $\beta_{qn}[m]$ is defined as $\beta_{qn}[m] = \beta_{qn}[m-1] + f(\hat{\alpha}_n[m])$ with $\beta_{qn}[-1] = 0$. Our fixed-point simulations show that the word length of β_{in} and β_{qn} has a significant impact on the output statistics. Using bit-true simulations we found that the $Q(22, 15)$ format provides enough accuracy. The $2 \times L \times N$ values of β_{in} and β_{qn} are stored in $RAM \beta$, as shown in Fig. 8. Also, the $Cos Module$ is used to calculate the $g(x)$ function using look-up tables. The first quarter cycle of the cosine function is quantized into 1024 segments and the resulting values are stored in one BRAM. The value of $g(x)$ over $(0, 1)$ is calculated from these stored values by exploiting the symmetry of the cosine function. The outputs of the $Cos Module$ are accumulated to compute the scaled values of (5) and (6), which are then stored in $RAM c$.

(3) Interpolation: In this step, fading samples generated at the reduced rate \hat{F}_s are oversampled and interpolated I times to provide samples at the target sample rate $F_s = I \times \hat{F}_s$. The interpolator requires the discrete difference between two consequent low-frequency samples $y[mI]$ and $y[(m+1)I]$, where $m = 0, 1, \dots$, to compute the interpolated signal. The interpolator generates the fading samples $y[mI + i]$, where $i = 0, 1, \dots, I-1$, as follows:

$$y[mI + i] = \frac{(y[(m+1)I] - y[mI])i}{I} + y[mI] \quad (7)$$

To avoid the multiplication and division operations, I is chosen to be a power of two. Also, we use an accumulator to implement (7) as follows:

$$y[mI + i] = \sum_{j=0}^i \frac{y[(m+1)I] - y[mI]}{I} + y[mI]. \quad (8)$$

The interpolator in Fig. 8 contains a 24-bit accumulator and one register that holds the input signal for an interval of I samples. Note that every stream of in-phase and quadrature samples requires a separate instantiation of the interpolator. Thus for an L -path simulator, $2L$ interpolators are required. A decoder selects which interpolator branch should store the present output sample from *RAM c*. The interpolator generates the final L streams of independent complex Rayleigh fading samples.

An important property of the proposed architecture is that since the same datapath is shared to update sinusoid parameters and to superimpose sinusoids, the number N of sinusoids mainly impacts the size of the memories used to store the sinusoid parameters. The computational complexity is directly proportional to the number L of independent faders. For example, a fading simulator with $L = 32$ paths, which requires 64 independent interpolators for the in-phase and quadrature components, uses only 6899 (7%) of the configurable slices, 10 (2%) of the BRAMs, and 1 ($< 1\%$) of the dedicated DSP48s on a Xilinx Virtex-4 XC4VLX200-11 FPGA while generating $32 \times 201 \times 10^6$ complex fading samples per second. The synthesis results show that 6214 out of 6899 (i.e., 90%) configurable slices used for the entire fading channel simulator are used by the interpolator. Since a time-multiplexed datapath is used to generate fading variates at a lower rate, for a Rayleigh fading channel simulator with a given F_s and f_D , there is an upper bound on the number N of sinusoids and the number L of paths. Assuming that $64 \times f_D \leq \hat{F}_s < 128 \times f_D$, one can see that

$$\log I = \lfloor \log_2(F_s/f_D) \rfloor - 6 \quad (9)$$

where $\hat{F}_s = 2^{-\log I} \times F_s$. Since $L \times N \geq 2^{\log I}$, using (9) we can write

$$2^{\lfloor \log_2(F_s/f_D) \rfloor} \geq 64 \times L \times N$$

With the approximation $\lfloor \log_2(F_s/f_D) \rfloor \approx \log_2(F_s/f_D) - 1$, we can write

$$L \times N < \frac{F_s}{128 \times f_D} \quad (10)$$

Equation (10) shows that one can increase the number L of independent paths and/or the number N of sinusoids for greater accuracy as long as the datapath for generating the fading variates at the lower rate \hat{F}_s has sufficient clock cycle budget $F_s/(128 \times f_D)$.

For a comparison with our best previous FPGA-based designs, we implemented the fading channel simulator with different numbers L of paths on a Xilinx Virtex-II Pro XC2VP100-6. The characteristics of our trial implementations are shown in Table I. This results show that the proposed

TABLE I
CHARACTERISTICS OF DIFFERENT RICEAN FADING CHANNEL SIMULATORS

Model	[21]	[24]	[14]	This Work	This Work
Paths L	32	32	16	32	64
Sinusoids N	8	8	8	32	32
Clock (MHz)	201	201	203	238	238
Output rate	32×201	32×201	16×203	32×238	64×238
Slices	97%	87%	32%	15%	29%
Mults.	66%	36%	64%	0.2%	0.2%
BRAMs	65%	79%	48%	2.0%	2%

design is significantly smaller and faster than our previous designs, while utilizing a greater number N of sinusoids to achieve more accurate fading variates. For example, compared to our previous implementation in [24], our new Ricean channel implementation accommodates twice as many paths L on the same FPGA, utilizes four times the number of sinusoids N for improved accuracy, increases the fading sample generation rate more than twice, utilizes three times fewer configurable slices, uses 180 times fewer dedicated multipliers, and requires at least 39 times fewer on-chip block memories. The increased compactness is mainly due to the time-multiplexed update procedure for the RWPs and also the use of a shared datapath for superimposing the sinusoids. Higher throughput is achieved by using the linear interpolators. Among various MIMO prototype implementations on FPGAs, to the best of our knowledge, only a few of them reported the characteristics of the implemented fading channel simulators. For example, the implementation of a (4, 4) MIMO channel on an Altera APEX EP20K1000EBC652-3 in [15] uses 58% of the logical elements and 17% of the memory bits while clocking at 50 MHz. Also, the design in [19] can support MIMO channels with no more than 16 delay paths and the fading sample generation rate is only three million samples per second. The design in [19] uses 25% of the logic elements, 40% of the on-chip memory, and 80% of the DSP blocks on the Altera Stratix-II FPGA. By comparing with these implementation results, one can see that our proposed channel simulator is significantly more compact and faster than these previous designs.

Note that the sample rate of the new fading simulator depends on the maximum speed of the interpolator stage if different clock sources are used for the first stage (i.e., generating fading samples at \hat{F}_s) and the second stage (i.e., the interpolator). For example, the interpolator in the proposed fading channel simulator on a Xilinx Virtex-II Pro XC2VP100-6 FPGA (for both the $L = 32$ and $L = 64$ cases) runs at 243 MHz. Thus the final fading sample generation rate is $L \times 243$ complex-valued fading samples per second.

V. CONCLUSIONS

Using a hardware-accelerated baseband channel simulator is an attractive way of avoiding the inconvenience and cost of field trial measurements while still permitting the accurate and repeatable characterization of wireless systems. We utilized an improved sum-of-sinusoid (SOS) based model that en-

ables accurate implementations of Rayleigh and Ricean fading channel simulators. We proposed a new updating procedure for the sinusoid parameters of the SOS-based fading model, which allows a significantly more compact implementation of a high path count Rayleigh and Ricean fading channel simulator. We also presented a reconfigurable architecture for the fading channel simulator that has a significantly higher fading variate generation rate compared to previous simulator designs. The new design utilizes time-multiplexed resource sharing to achieve a compact implementation and a simple linear interpolator that produces the samples at the full output rate. Within a single Xilinx Virtex-4 XC4VLX200-11, up to 448 different Rayleigh channels can be implemented, generating 448×190 million complex fading variates per second. Being able to implement an entire frequency-selective MIMO fading channel simulator on a small fraction of a single FPGA allows designers to prototype the transmitter and receiver on the same FPGA and then allow their performance to be verified under a wide variety radio propagation scenarios.

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